EXAMINER'S AMENDMENT

1. This action is responsive to appeal brief filed on Feb. 9, 2009.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Joseph Ryan on May 15, 2009.

The application has been amended as follows:

Claim 1 (Currently amended): A network processor integrated circuit comprising:

a plurality of processor clients internal to the network processor integrated circuit;

an internal memory having a plurality of memory instances; and

an internal memory controller for controlling access of the plurality of processor clients to the plurality of memory instances, the internal memory controller comprising a configurable switching element;

the configurable switching element being connectable between the plurality of processor clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of processor clients to particular ones of the plurality of memory instances;

wherein the configurable switching element is configurable to connect any one of at least a subset of the plurality of processor clients to each of at least a subset of the plurality of memory instances,

such that in a first selectable configuration of the configurable switching element, a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in a second selectable configuration of the configurable switching element, the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set;

wherein a different set of mask bits is associated with each of a plurality of different memory instance sizes, and a different address decoder value is associated with each of the plurality of memory instances;

wherein address decoding logic applies the mask bits for a given memory instance to an incoming address from the given processor client, and compares the result to the address decoder value for the given memory instance to determine if the incoming address is directed to an address in the given memory instance.

Claims 13-14: canceled.

Claim 15: replace "14" after "integrated circuit of claim" with -1-- in line 1.

Claim 20 (currently amended): A method for use in a network processor integrated circuit for controlling access of a plurality of processor clients internal to the network processor integrated circuit to a plurality of memory instances of an internal memory of the network processor integrated circuit, the method comprising the steps of:

providing within the network processor integrated circuit an internal memory controller comprising a configurable switching element;

the configurable switching element being connectable between the plurality of processor clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of processor clients to particular ones of the plurality of memory instances;

wherein the configurable switching element is configurable to connect any one of at least a subset of the plurality of processor clients to each of at least a subset of the plurality of memory instances; and

selecting one of at least a first selectable configuration and a second selectable configuration of the configurable switching element, wherein in the first selectable configuration a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in the second selectable configuration the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set;

wherein a different set of mask bits is associated with each of a plurality of different memory instance sizes, and a different address decoder value is associated with each of the plurality of memory instances;

wherein address decoding logic applies the mask bits for a given memory instance to an incoming address from the given processor client, and compares the

result to the address decoder value for the given memory instance to determine if the incoming address is directed to an address in the given memory instance.

REASONS FOR ALLOWANCE

3. Claims 1-12, 15, 16 and 20 are allowable over the prior art of record.

4. This communication warrants no examiner's reason for allowance, as applicant's reply makes evident the reason for allowance, satisfying the record as whole as required by rule 37 CFR 1.104 (e). In this case, the substance of applicant's remarks in the appeal brief, pages 8-12 and 15-16, filed on Feb. 9, 209 with respect to the claim limitations point out the reason claims are patentable over the prior art of record. Thus, the reason for allowance is in all probability evident from the record and no statement for examiner's reason for allowance is necessary (see MPEP 13202.14).

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUSSEIN A. EL CHANTI whose telephone number is (571)272-3999. The examiner can normally be reached on Mon-Fri 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hussein Elchanti/
Patent Examiner

May 15, 2009